

TUTORIAL PROPOSAL for VLSI 2011: Advanced Analog-Mixed Signal Circuit Techniques

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Abstract: This tutorial begins with a broad overview of challenges in emerging mixed signal systems. After describing the system-level requirements along with the architecture and circuit needs, specific circuit and system solutions will be discussed to highlight promising approaches. Design techniques for advanced analog- and mixed signal circuit blocks such as phase-locked loops and analog-to-digital converters will be covered in detail. Finally, the modeling and analysis of substrate noise coupling in mixed-signal integrated circuits is addressed.

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Target Audience: Analog and mixed signal designers from industry with a basic background in circuit design. Graduate students who wish to gain a deeper knowledge of this area.

Keywords: Mixed-signal systems, sensor networks, solar electronics, phase-locked loops, data converters, substrate noise, macro-modeling.

Detailed program: This day long tutorial addresses both the system- and circuit-level aspects of emerging mixed-signal systems. Analysis and design techniques to implement analog to digital converters, phase-locked loops, and the impact of substrate noise on these circuits in large system-on-chips will be discussed. The tutorial is categorized into the following four categories.

1. Challenges in Emerging Mixed-Signal Systems and Applications (1.5Hrs)

With the successful integration of systems-on-a-chip for a wide range of ubiquitous applications including cell phones and gaming devices, new applications for SOCs are arising that create unique challenges at the circuit and system level. In this talk several emerging applications for integrated mixed-signal systems will be highlighted including sensor networks, solar electronics, and tracking and monitoring devices. The system level requirements will be discussed along with the architecture and circuit needs. Specific circuit and system solutions will be discussed to highlight promising approaches to address both application and process challenges in the coming decade.

2. Substrate Noise in Mixed-Signal Systems (1.5Hrs)

With the high levels of integration in current and future generations of Systems on a Chip (SoCs), noise coupling from the digital circuitry to the sensitive analog and RF circuits is an important concern for ensuring first-pass silicon. In this tutorial the modeling and analysis of substrate noise coupling in mixed-signal integrated circuits is addressed. High accuracy substrate modeling, efficient substrate macromodels, efficient digital noise simulation, and model parameter extraction will be described. This will be followed with measured results and the impact of substrate noise coupling in typical circuit building blocks (low noise amplifier, ring oscillator, delta-sigma modulator, and phase-locked loop).

3. Phase-Locking Techniques for Frequency Synthesis (1.5Hrs)

Phase-locked loops (PLLs) are essential building blocks in all digital, analog, and radio-frequency integrated circuits (ICs). The noise, power, and area of PLLs determine many of the key performance parameters in all such ICs. This tutorial describes the fundamental principles and concepts of PLL design. After reviewing the operation of a simple type-1 PLL and the characteristics of its building blocks, the operating and design principles of a charge-pump PLL will be discussed in detail. Phase noise analysis using a small-signal model will be described and noise-bandwidth-power tradeoffs will be presented. Existing and emerging techniques to alleviate these tradeoffs will be briefly discussed.

4. Advanced and Emerging ADCs (1.5Hrs)

Many analog IC designers and students are drawn to ADCs. While some ADC realizations have had a lasting impact, examples including pipelined ADCs with digital redundancy, flash ADCs with folding and interpolation, and multi-bit delta-sigma modulators with dynamic element matching, there are many more recent, advanced and emerging ADC design techniques that are receiving much attention and also gaining momentum in some areas. Many of these ideas are showered with doubts and honest criticism. However, we may also be entering a new era where some of these developments would help resolve the toughest submicron scaling challenges that analog designers face today. This tutorial will

summarize and ponder the impact of a few selective as well as random slices of these advanced and emerging ADC designs.

Presenter Biographies

Terri S. Fiez is Head of Electrical Engineering and Computer Science at Oregon State University. From 2008 until mid 2009 she co-founded and served as CEO of Azuray Technologies, a startup developing micro-inverters for solar applications. Since returning to OSU in September 2009, she has taken on a leadership role for OSU's Sustainable Energy and Infrastructure (SENERGI) research thrust. She has been very active professionally as a researcher in analog and mixed-signal IC design and innovative engineering education approaches, serving on the ISSCC executive committee, as associate editor of TCASII, and as a member of the administrative committee for the Solid-State Circuits Society. Dr. Fiez has published more than 100 technical papers and advised more than 70 graduate students in her career and she is an IEEE Fellow and was previously awarded the National Science Foundation's Young Investigator Award and the IEEE Education Activities Board Innovative Education Award. After receiving her Ph.D. from OSU in 1990 she was a faculty member at Washington State University before returning to OSU to lead the department in 1999.

Kartikeya Mayaram is currently a Professor in the School of Electrical Engineering and Computer Science at Oregon State University. He is an IEEE Fellow and a recipient of the NSF Faculty Early Career Development Award. After receiving his Ph.D. from the University of California, Berkeley he worked at Texas Instruments and Bell Labs prior to joining academia. His research interests are in simulation, modeling, substrate noise coupling in mixed-signal circuits, and analog/RF design.

Pavan Kumar Hanumolu received the Ph.D. degree in electrical engineering from Oregon State University in 2006. Currently, he is an Assistant Professor in the School of Electrical Engineering and Computer Science at the same University. His research interests include high-speed I/O interfaces, digital techniques to compensate for analog circuit imperfections, time-based signal processing, and power-management circuits.

Un-Ku Moon has been with the Oregon State University since 1998. Prior to that, he was with Bell Labs (Reading & Allentown) 1988-1989 and 1994-1998. He received a bachelor's degree from the University of Washington, a master's degree from Cornell University, and a Ph.D. from the University of Illinois, Urbana-Champaign. His current research activities are found at <http://eecs.oregonstate.edu/~moon/research>.

Tutorial material to be given to participants: The presentation slides will be made available to the participants.